TWO STAGE DUAL GATE MESFET MONOLITHIC GAIN CONTROL AMPLIFIER FOR KA-BAND*

by

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ABSTRACT

A monolithic two stage gain control amplifier has been developed using submicron gate length dual gate MESFETs fabricated on ion implanted material. The amplifier has a gain of 12 dB at 30 GHz with a gain control range of over 30 dB. This ion implanted monolithic IC is readily integrable with other phased array receiver functions such as low noise amplifiers and phase shifters.

INTRODUCTION

The use of GaAs dual gate FETs for gain control in microwave amplifiers has been well known for nearly fifteen years [1,2]. Examples of such circuits have been demonstrated in numerous hybrid and monolithic implementations ranging in application and frequency of operation from television receivers at UHF, to 20 GHz variable power amplifiers for satellite communications [3,4,5]. In this paper we show the feasibility of employing dual gate FETs (DGF's) in monolithic gain control amplifiers (GCA's) at 30 GHz using ion implanted devices with e-beam defined sub half-micron gates.

Specifically, the application is for 30 GHz GCA's to be used in receivers of a ~400 element feed array in an advanced satellite antenna system [6]. The antenna is a dual reflector offset Cassegrain system that achieves electronic beam steering (as well as multiple spot beams) by electronically shifting the focal point (points) on the feed array. A focal point is defined by a cluster of about twenty activated receivers having a specific gain and phase distribution across the cluster [7]. The GCA's are used to achieve the required gain distribution across any one cluster as well as for on and off control to allow definition of a specific 20-element cluster. Requirements for these GCA's include five levels of gain control in the range +12dB through -1dB with minimum associated phase shift, and an off state. Since the GCA's are used for post-amplification only, noise figure characteristics are not critical. The GCA's are to cover the 27.5-30 GHz frequency range.

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DEVICE AND CIRCUIT DESIGN

The low frequency maximum available gain (MAG) of a DGF with its second gate RF-grounded is greater than its single gate counterpart and falls off at a rate of 6 dB/octave. However, as discussed in References [2] and [8], at high frequencies the device parasitic elements cause MAG to fall at a greater rate with frequency. Consequently, to extend the useful operating range of such devices, attention must be given to proper device design which includes scaling of the device geometry with frequency. As discussed in an earlier paper [9], of particular importance is the low inductance (and separate) RF grounding of the second gate to prevent unwanted feedback. Furthermore, to have adequate gain at Ka-band, sub half-micron gates are required.

The DGF used in the monolithic amplifier design is identical to the dual gate device described in [9]. Each (2)x100x0.3 micron DGF has an on-chip 1.7 pF silicon nitride MIM bypass capacitor connecting the second gate to a grounding pad. The S-parameters were measured for a single discrete DGF, including the on-chip capacitor, in the frequency range 2-26 GHz, to characterize the devices for amplifier design. Bias was chosen for maximum gain (V_D=5.0V, I_D=15mA, V_{G1}=0, V_{G2}=0.5V). To ensure adequate bypass at lower frequencies, an external 47 pF capacitor was connected from the second gate (in parallel with the 1.7 pF cap) to ground. Using this measured data, a DGF equivalent circuit consisting of a cascode connection [2] of two single gate FETs was developed. The equivalent circuit element values were adjusted, using EEsof's Touchstone optimization program, to fit the calculated S-parameters to the measured data over the 2-26 GHz band. Figure 1 shows the equivalent circuit. For amplifier design the DGF equivalent circuit was extended to Ka-band by eliminating the 47 pF capacitor and calculating the S-parameters in the band of interest. Figure 2 shows the calculated MAG (or MSG for K<1) in the 20-40 GHz frequency range. Note that for f<35 GHz, the stability factor, K, is less than 1. At 40 GHz MAG is 8 dB.

A two stage design was chosen for at least two reasons. By distributing the gain control over two stages the total associated phase shift is reduced since phase shift in DGF's is minimum near the top of the gain control range. In a similar way noise figure degradation is minimized by avoiding large gain changes in either stage. The complete two stage amplifier IC is shown in

Figure 3. Gain is adjustable at both stages by controlling the dc voltage applied to the second gates. The monolithic IC amplifier includes input, output, and interstage matching networks as well as interstage coupling capacitors. The chip dimensions are 1.83 x 0.51 x 0.15mm^3. Some provision for modification of the input and output matching networks is also included on chip.

One of the characteristics of the dual gate FET is its high output impedance. For the 100 micron device the magnitude of the output S-parameter, S_{22}, is nearly unity and significant mismatch must be employed in the output and interstage networks to achieve reasonably flat gain over the desired bandwidth. This fact, coupled with the impedance restrictions associated with monolithic design (high impedance transmission lines are limited to $Z_o \leq 100$ ohms), restrict the fractional bandwidth to about 10%. Larger gate widths can reduce this problem at the expense of increased power consumption. The predicted performance of the two-stage amplifier (gate 2 adjusted for maximum gain) is 8 dB $\pm$ 2 dB across the 27.5-30 GHz band. To allow for processing variations in the device parameters, some of the high impedance lines in the amplifier layout are provided with design alternatives, i.e., the length of lines can be easily changed to another fixed length by a simple bonding operation.

IC FABRICATION

The gain control ICs were fabricated using a hybrid e-beam/optical lithography process described previously [9]. Fabrication of these ICs will soon be transferred to a hybrid e-beam/optical stepper process which uses direct-write e-beam only for the gate level and optical projection lithography for all other levels.

The amplifiers are fabricated on ion implanted LEC substrate material with a 6 x 10^{12} cm^{-2}, 120 KeV silicon implant. A dc drain I-V and SEM of the gate area are shown in Figures 4a and 4b. A significant problem encountered in the fabrication of these dual gate devices was difficulty with adhesion of the thin strip of resist separating the two gate openings, to the GaAs substrate, during the recess etch. Several recess etches were tried before it was discovered that a phosphoric acid based etch did not cause separation of the thin resist strip and also provided good adhesion of the gate metalization.

RF RESULTS

After thinning (to 0.15 mm) and backside metallization, the wafers are scribed and die separated. The monolithic two stage GCA is soldered to a gold plated brass carrier block and inserted in an in-line waveguide compatible test fixture incorporating antipodal fin-line transitions. These transitions are similar to those described in an earlier paper [10]. They provide a low loss connection from the chip's 50 ohm input and output microstrip lines to standard Ka-band waveguide. The total insertion loss for the fixture is between 0.6 and 0.8 dB over the 26.5-37 GHz band.

Several GCA chips from different runs were evaluated at Ka-band. Figure 5 shows the superposition of the gain versus frequency characteristics for a GCA chip from our first run measured from 29 to 31 GHz. The second gate terminals of both DGF stages were connected to a common bias source, and the voltages chosen such as to achieve equal (3 dB) gain steps in Figure 5. A maximum gain of 12 dB occurs at 30 GHz with a 10$\pm$2 dB bandwidth of approximately 2 GHz for the monolithic amplifier with no circuit modification. With the second gate voltage ranging from -0.6V to about -4V, more than 30 dB of gain adjustment is possible.

To obtain operation over the required bandwidth of 27.5-30 GHz, two minor modifications were made in the interstage and output impedance matching networks. The 100 ohm high impedance lines were made electrically longer by adding about 0.15 mm bond wire in both networks. These modifications were made on our second run of GCA's. The resulting amplifier response for different gain levels is shown in Figure 6. A maximum gain of 12 dB is obtained at mid-band with a 2 dB bandwidth of about 2 GHz. The corresponding common second gate voltage ranges from -0.24V to -1.86V. Figure 7 shows the measured insertion phase response across the same band. Note that for the required gain adjustment of +12 dB to -1 dB the phase variation is no worse than about $\pm$15 degrees at center band. The measured noise figure was 16 dB at maximum gain and 19 dB at the -1 dB attenuation level.

CONCLUSIONS

A GaAs monolithic two-stage gain control amplifier using dual gate FETs has been demonstrated for the first time at Ka-band. The FETs incorporate dual 0.25 x 100 micron gates and are fabricated on ion-implanted material. Circuit design was based on modeled S-parameters that were fitted to measured data obtained on discrete transistors over the 2-26 GHz frequency range. The model was then used to extrapolate the S-parameters to the 20-40 GHz range.

Due in part to monolithic circuit design constraints and the requirement for minimum power consumption (i.e., larger gatewidth FETs are undesirable) the predicted amplifier fractional bandwidth is limited to about 10%. Actual fabricated two-stage amplifiers exhibit fractional bandwidths of 5 to 7%. However, due to processing variations and limitations in the accuracy of the measured S-parameters the center frequency of the actual amplifiers are in error by the same order as the measured bandwidths. Consequently, some post fabrication circuit adjustments must be made to obtain useable amplifiers in the band of interest. Nevertheless, it has been shown that such adjustments can be made, and that gain control amplifier characteristics at 30 GHz are similar to corresponding amplifiers at lower microwave frequencies.

Future work will be directed toward obtaining wider bandwidth designs (possibly at the expense of greater power consumption), more accurate device modeling, and better processing control.

These efforts should lead to monolithic Ka-band GCA's with fractional bandwidths of at least 10% and operating in the specified 27.5-30 GHz band with no circuit modifications required. The feasibility of using such amplifiers for feed array receiver applications for future satellite communication systems has been demonstrated.

ACKNOWLEDGEMENTS

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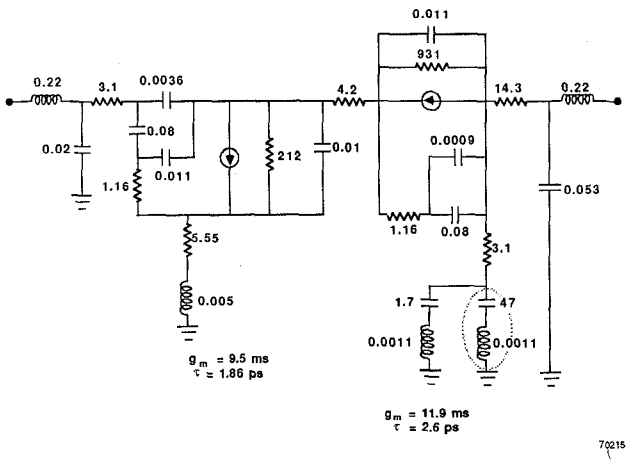

Figure 1. Equivalent Circuit Derived from Measured S-Parameters for 2x(100x0.3) Micron Dual Gate FET.

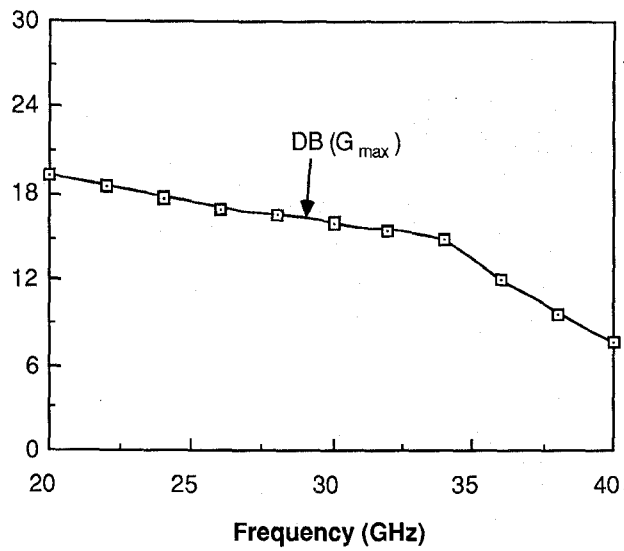

Figure 2. Maximum Available Gain/Maximum Stable Gain for FET of Figure 1.

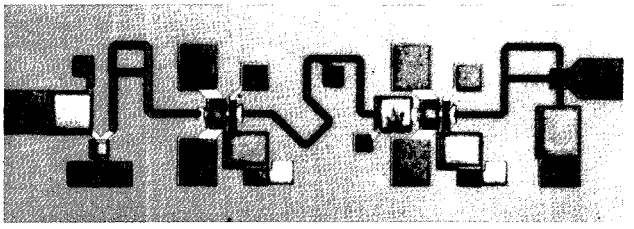

Figure 3. Two-Stage Monolithic Gain Control Amplifier Chip Dimensions: (1.8x0.5x0.15) mm.

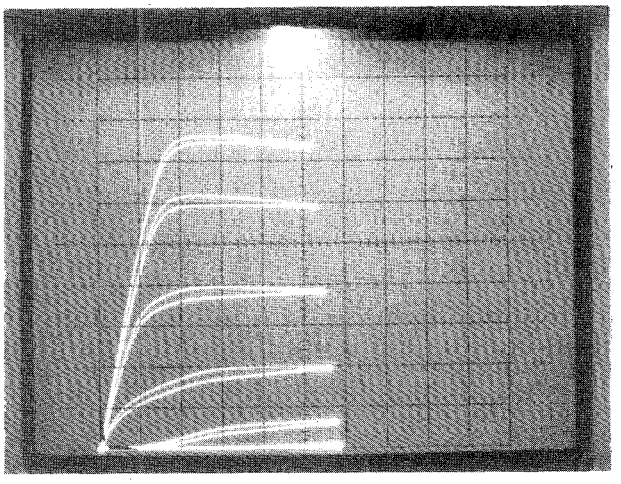

Figure 4a. DC Output Characteristics for Dual Gate FET [Vert:I_d = 5mA/div; Horiz:V_d = 1V/div; Step Size:V_g = 1V].

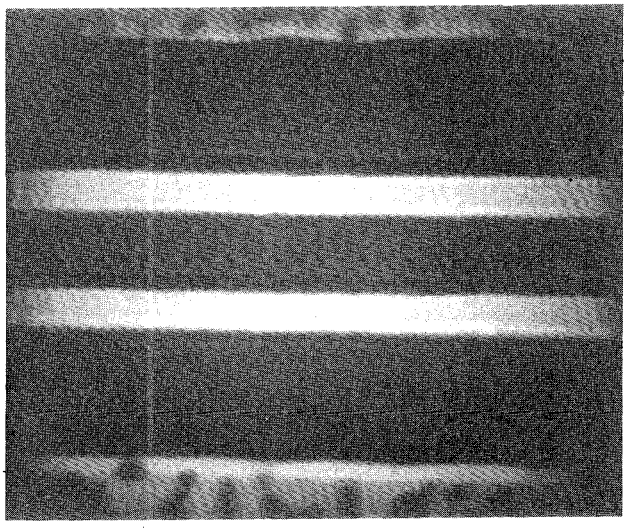

Figure 4b. SEM Photo of Gate Area; Magnification: 30K.

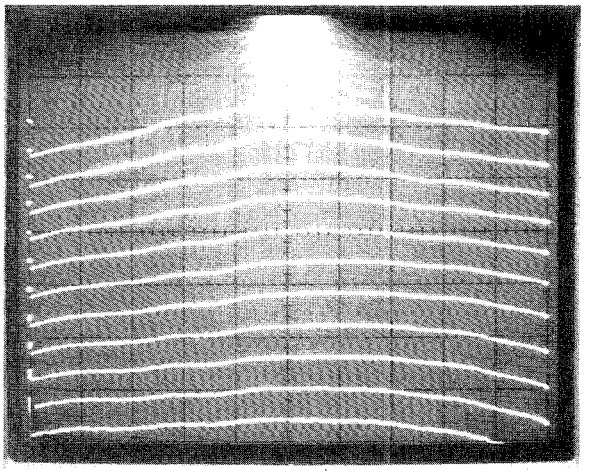

Figure 5. Gain vs. Frequency for Unmodified Gain Control Amplifier [Vert:G = 5dB/div; Horiz: 200 MHz/div, 29-31 GHz; Ref-Center Line].

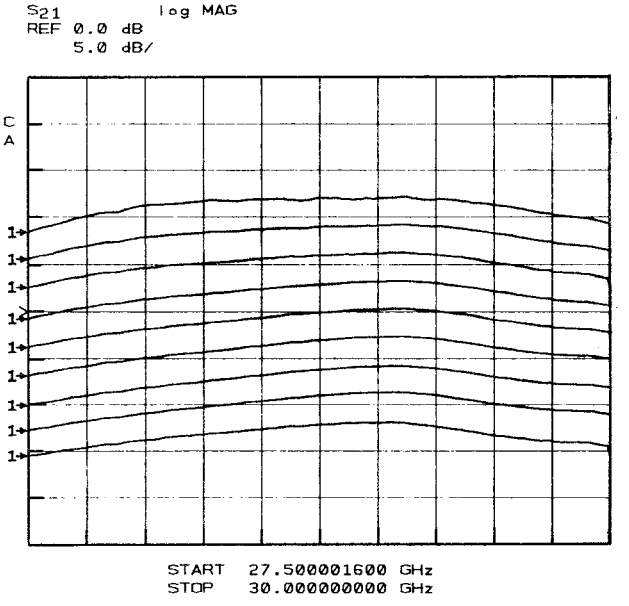

Figure 6. Gain vs. Frequency for Modified Gain Control Amplifier [Vert:G = 5 dB/div; Horiz: 250 MHz/div, 27.5-30 GHz; Ref-Center Line].

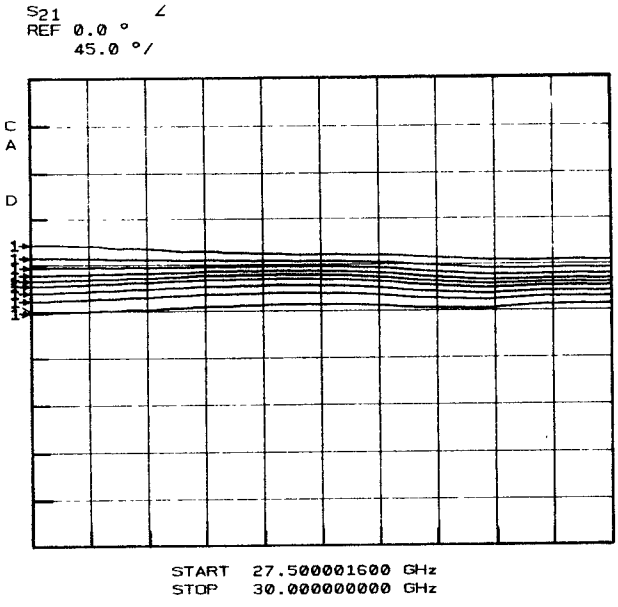

Figure 7. Associated Relative Phase Shift for Modified Gain Control Amplifier [Vert: 45^{o}/div; Horiz: 250 MHz/div, 27.5-30 GHz].